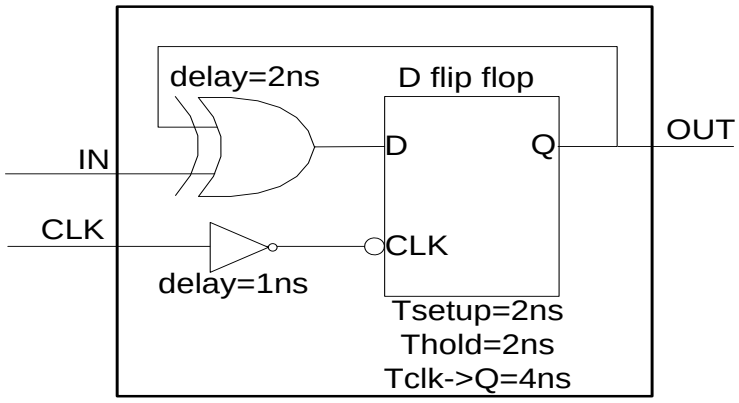
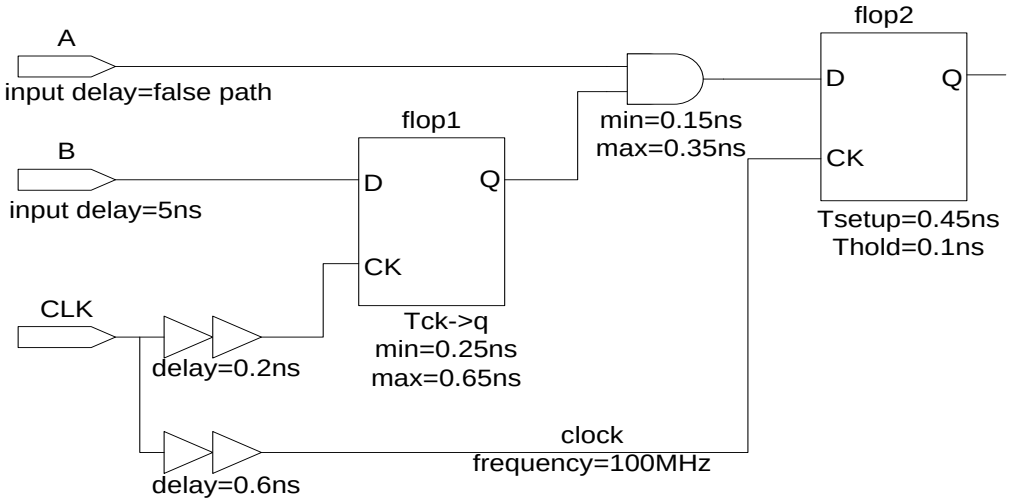
Given the following design



1. What are the effective setup and hold times for the following circuit?
   A. T_{setup} = 4 ns, T_{hold} = 1 ns
   B. T_{setup} = 3 ns, T_{hold} = 0 ns
   C. T_{setup} = 3 ns, T_{hold} = 1ns
   D. T_{setup} = 2 ns, T_{hold} = 0 ns
2. What is the maximum operating frequency of the above circuit?
   A. 250 MHz
   B. 80 MHz
   C. 125 MHz
   D. 166.7 MHz
3. What does the above circuit function as?
   A. D flip flop with enable
   B. T flip flop
   C. JK flip flop
   D. SR flip flop
4. Which equation best describes the maximum clock frequency in a synchronous system
   A. Max Freq = 1/(Tprop_delay + Tsu + Thold)
   B. Max Freq = 1/(Tprop_delay + Tsu + Tco + Thold)
   C. Max Freq = 1/(Tsu + Tco + Thold + Tclock_skew)
   D. Max Freq = 1/(Tprop_delay + Tsu + Tco + Tclock_skew)
   E. Max Freq = 1/(Tprop_delay + Tsu + Thold + Tco + Tclock_skew)
5. Which one of the following could more likely cause soft error in memory element?
   A. Cosmic particles
   B. IR drop
   C. Ground bounce
   D. Cross talk



6. What is the setup margin for flop2?
   A. 8.95ns
   B. 9.55ns
   C. 0.85ns
   D. 7.75ns
7. What is the hold margin for flop2?
   A. 0.5ns
   B. 0.1ns
   C. -0.10ns
   D. 9.9ns